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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,855	03/29/2005	Nicola Da Dalt	10808/172	6363

7590 10/04/2005
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EXAMINER

ARENA, ANDREW OWENS

ART UNIT PAPER NUMBER

2811

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/511,855		DA DALT, NICOLA	
	Examiner		Art Unit	
	Andrew O. Arena		2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 October 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>10/14/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 7 recites "a metal plate electrically connected to one of the crossing points in a latticed region of the first and second substructure" which is unclear, since connecting to both the first and second would short-circuit the structure and eliminate capacitance. It seems the underlined "and"s in lines 4 and 6 of claim 7 should be changed to "or"s. Claim 7 is also written in an overall unclear manner, it is difficult to read the language of claim 7 onto applicants Fig 3. It seems applicant means to claim "a metal plate electrically connected to either the crossing points in a latticed region of the first substructure and the electrically conductive regions of the second substructure or the crossing points in a latticed region of the second substructure and the electrically conductive regions the first substructure, by means of one or more respective via connections." It seems the "or" in line 5 should be changed to an "and". Also, the second "of" in line 6 should be changed to an "or". Appropriate correction is required.

Claim Rejections - 35 USC § 103

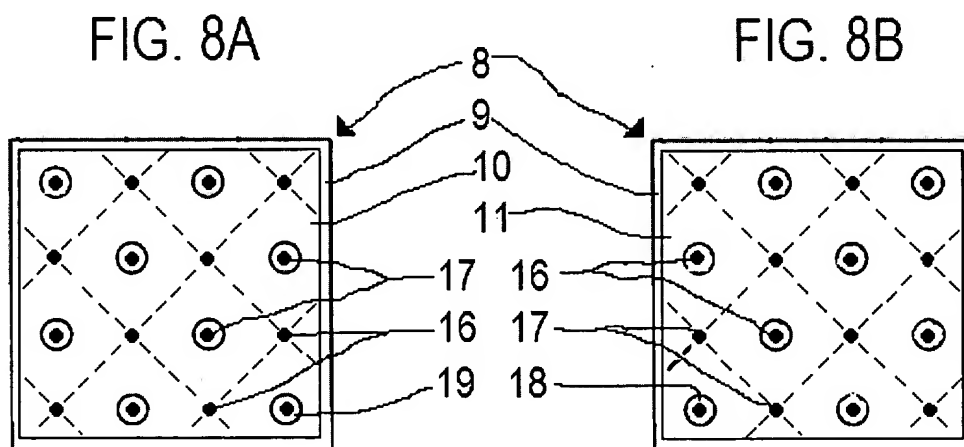
Art Unit: 2811

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arita et al. (US 6,046,467) – hereinafter Arita – in view of Kuroda et al. (US 6,370,010) – hereinafter Kuroda.

3. Reference is made to the structure of Kuroda Fig 8, which is based on Figs 1-4 (col 8 ln 30-35, col 5 ln 58-59). Fig 8 is analogous to Fig 1, but there are no analogous drawings to Figs 3-4. Examiner has drawn and attached Figs 8A and 8B, which correspond to Figs 3A and 3B, for ease of reference in this rejection. In a similar manner, it is easy to picture the drawing corresponding to Fig 4, which is not shown.



4. Regarding claim 1, Arita discloses (Fig 1) a semiconductor component (col 2 ln 53) comprising a semiconductor substrate (21; col 2 ln 59) having an insulating layer

Art Unit: 2811

(21a+26; col 2 ln 58-59, col 3 ln 31-34) on the semiconductor substrate and having a capacitance structure (25; col 3 ln 2-4) in the insulating layer, wherein the capacitance substructures (22-24) are parallel to the substrate surface, but discloses a conventional parallel plate capacitor, not the claimed capacitance structure. Kuroda teaches a capacitance structure (Fig 8; col 8 ln 30-35) that comprises:

a first substructure (Fig 8A: 10; col 6 ln 9) which has a first cohesive latticed (represented by dashed lines) region which extends in a first common plane (Fig 8A: 10; Fig 4) such that it has common top and bottom surfaces which limit the first cohesive latticed region in each of its subregions (diamond outlined by dashed lines) from above and from below; and

a first substructure having electrically conductive regions (Fig 8A: 17; col 6 ln 62-63) arranged in cutouts (Fig 8A: 19; col 7 ln 21) in the first cohesive latticed region of the first substructure at a distance from edge regions of the cutouts in the common plane, and

wherein the electrically conductive regions comprise node points between via connections (Fig 8A: 17; col 7 ln 21).

5. Further regarding claim 1, Kuroda does not expressly disclose the cohesive latticed region is metal. However, it would have been obvious to a person of ordinary skill in the art at the time of the invention to form the cohesive latticed region (Fig 8A: electrode 10; col 6 ln 9) from metal; at least because it is a common electrode material.

6. Further regarding claim 1, Kuroda discloses wherein the first cohesive latticed region is electrically connected to the first electrode (col 6 ln 60-63), but does not

Art Unit: 2811

expressly disclose connection to a "first connecting line". Kuroda discloses wherein the electrically conductive regions are electrically connected to the second electrode (col 6 ln 63-67), but does not expressly disclose connection to a "second connecting line". It would have been obvious to a person of ordinary skill in the art at the time of the invention to form the claimed connections; at least for the purpose of connecting and using the capacitor.

7. Further regarding claim 1, the field of endeavor is capacitor structures for both Arita and Kuroda. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to form the capacitor of Arita with the capacitance structure taught by Kuroda; at least for the purpose of achieving a very low equivalent series inductance (ESL: Kuroda col 3 ln 19-21).

8. Regarding claim 2, Kuroda discloses wherein the capacitance structure further comprises a second substructure (Fig 8B: 11; col 6 ln 9-10) parallel to and at a distance from the first substructure (col 6 ln 6-10; Fig 4, 8A) wherein the second substructure comprises a second cohesive latticed metal region (dashed lines in Fig 8B) which extends in a second common plane (11; Fig 4, 8A) parallel to the substrate surface such that it has common top and bottom surfaces which limit the second latticed metal region in each of its subregions from above and below, and wherein the first and second substructures are electrically connected (17 forms the electrically conductive region of the first substructure and electrically connects (col 6 ln 60-67) to the second cohesive latticed metal region 11 of the second substructure).

9. Regarding claim 3, Kuroda discloses wherein the second substructure is of the same design as the first substructure (col 6 ln 12-19), and the first and second substructures are arranged offset from one another (col 6 ln 15; lattices are clearly offset in Figs 3A&3B and 8A&8B) such that the electrically conductive regions (17; Fig 8A) of the first substructure are arranged vertically above (corresponding to Fig 4) crossing points in the second cohesive latticed metal region (17; Fig 8B) of the second substructure, and crossing points (16; Fig 8A) in the first cohesive latticed metal region of the first substructure are arranged vertically above (Fig 4) electrically conductive regions (16; Fig 8B) of the second substructure.

10. Regarding claim 4, Kuroda discloses wherein the crossing points (16; Fig 8A) in the first cohesive latticed metal region of the first substructure are electrically connected to the electrically conductive regions (16; Fig 8B) of the second substructure (col 6 ln 60-63), and the electrically conductive regions (17; Fig 8A) of the first substructure are electrically connected to the crossing points (17; Fig 8B) in the second cohesive latticed metal region of the second substructure (col 6 ln 64-67), by means of at least on respective via connection (16&17; col 6 ln 60, 63).

11. Regarding claim 5, Kuroda discloses wherein the second cohesive latticed metal region of the second substructure is offset (col 6 ln 15; lattices are clearly offset in Figs 3A&3B and 8A&8B) from the first substructure so that the electrically conductive regions (17; Fig 8A) of the first substructure are arranged vertically above (corresponding to Fig 4) crossing points in the second cohesive latticed metal region (17; Fig 8B) of the second substructure.

12. Regarding claim 6, Kuroda discloses wherein the electrically conductive regions (17; Fig 8A) of the first substructure and the crossing points (17; Fig 8B) in the second cohesive latticed metal region of the second substructure are electrically connected (col 6 ln 64-67), by means of at least one respective via connection (16&17; col 6 ln 60, 63).

13. Regarding claim 7, examiner has interpreted this claim as "a metal plate electrically connected to the crossing points in a latticed region of the first substructure and the electrically conductive regions of the second substructure by means of one or more respective via connections." This is in accordance with applicants Fig 3. Kuroda discloses a metal plate (bottom most 10 in Fig 4) electrically connected (col 6 ln 60-63) to the crossing points (16; Fig 8A) in a latticed region of the first substructure (10) and the electrically conductive regions (16; Fig 8B) of the second substructure (11) by means of one or more respective via connections (16; col 6 ln 60-63).

14. Regarding claim 8, Kuroda discloses wherein the first cohesive latticed metal region has at least two round cutouts (Figs 3A&3B and 8A&8B).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2811

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven Loke
Primary Examiner

A handwritten signature in black ink, appearing to read "Steven Loke", written in a cursive style.